	L #	Hits	Search Text	DBs	Time Stamp
1	L6	998	(((threshold or channel$3) near4 (implant$6 or inplant$6)) same WELL$3) and ((MOSFET or CMOS or BICMOS or (metal adj oxide adj semiconductor adj field adj effect adj transistor) or (complementary adj metal adj oxide adj semiconductor))) and ((STI or LOCOS or (shallow adj trench adj isolation)))	USPAT	2005/01/17 13:53
2	L7	717	WELL$3 near8 bur$4 near8 (implant$6 or inplant$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
3	L11	1093	(P near2 base) near8 (WELL$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
4	L28	1098	epitaxial same locos	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53

	L #	Hits	Search Text	DBs	Time Stamp
5	L29	84	(halo or pocket) and (epitaxial same locos)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 16:58
6	L31	16	locos and epitaxial and church.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
7	L23	1	("5270265").PN.	USPAT; USOCR	2005/01/17 13:53
8	L25	1	("6015757").PN.	USPAT; USOCR	2005/01/17 13:53
9	L26	1	("6440640").PN.	USPAT; USOCR	2005/01/17 13:53
10	L27	1	("20020158283").PN.	US-PGPUB; USPAT; USOCR	2005/01/17 13:53
11	L22	44	(438/188).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53

	L #	Hits	Search Text	DBs	Time Stamp
12	L13	128	((threshold or channel$3) near4 (implant$6 or inplant$6)) same WELL$3 same ((MOSFET or CMOS or BICMOS or (metal adj oxide adj semiconductor adj field adj effect adj transistor) or (complementary adj metal adj oxide adj semiconductor))) same ((STI or LOCOS or (shallow adj trench adj isolation)))	USPAT	2005/01/17 13:53
13	L18	163	((P near2 base) near8 (WELL$3)) same (implant$4 or inplant$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
14	L19	133	(((P near2 base) near8 (WELL$3)) same (implant$4 or inplant$4)) and ((MOSFET or CMOS or BICMOS or (metal adj oxide adj semiconductor adj field adj effect adj transistor) or (complementary adj metal adj oxide adj semiconductor)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
15	L17	296	(438/276).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53

	L #	Hits	Search Text	DBs	Time Stamp
16	L21	222	(438/153).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
17	L15	433	(WELL$3 near8 bur$4 near8 (implant$6 or inplant$6)) and ((MOSFET or CMOS or BICMOS or (metal adj oxide adj semiconductor adj field adj effect adj transistor) or (complementary adj metal adj oxide adj semiconductor)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
18	L20	692	(438/199).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53
19	L24	781	(438/154).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 13:53

	L #	Hits	Search Text	DBs	Time Stamp
20	L14	870	((((threshold or channel$3) near4 (implant$6 or inplant$6)) same WELL$3) and ((MOSFET or CMOS or BICMOS or (metal adj oxide adj semiconductor adj field adj effect adj transistor) or (complementary adj metal adj oxide adj semiconductor))) and ((STI or LOCOS or (shallow adj trench adj isolation)))) not (((threshold or channel$3) near4 (implant$6 or inplant$6)) same WELL$3 same ((MOSFET or CMOS or BICMOS or (metal adj oxide adj semiconductor adj field adj effect adj transistor) or (complementary adj metal adj oxide adj semiconductor))) same ((STI or LOCOS or (shallow adj trench adj isolation))))	USPAT	2005/01/17 15:00
21	L32	623	(438/241).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 15:00
22	L33	745	(438/258).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 16:03

	L #	Hits	Search Text	DBs	Time Stamp
23	L34	1727	(438/297).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 16:54
24	L35	15	34 and 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 16:54
25	L36	19	34 and (halo or pocket)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/01/17 16:59

US-PAT-NO: 6342431

DOCUMENT-IDENTIFIER: US 6342431 B1

TITLE: Method for eliminating transfer gate sacrificial oxide

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Brief Summary Text - BSTX (5):
In processing a logic wafer, the initial step is forming an oxide (e.g., typically referred to as a "pad oxide"), and thereafter depositing a silicon nitride layer (e.g., typically referred to as a "pad nitride"), creating an isolation feature (e.g., a **shallow trench isolation,** but equally relevant to a field oxide isolation or other means of isolation), and filling the trench with insulator material.

Brief Summary Text - BSTX (8):
However, the above-described conventional method is problematic because the combination of these isotropic wet etches for removing the pad nitride, pad oxide, and TG Sac Ox consumes isolation oxides. In **STI** isolation, the weak points in the TEOS fill create problems for subsequent processing when exposed during prior processing.

Brief Summary Text - BSTX (9):
For example, trench isolation wafers (e.g., **STI**) are scrapped for defects called "seams", which also cause polysilicon-polysilicon features to short electrically. In high aspect ratio isolation trenches, a filling void occurs during the trench fill process which, if exposed to wet etches (particularly oxide etches), creates an indentation in which the seams defect can form. Thus, additional stripping steps result in high product costs due to defective parts. Field oxide isolation processing also has certain defects associated

therewith including oxide consumption, leakage, poor insulation and a "corner
device".

Brief Summary Text - BSTX (18):
An important feature of the process of the present invention is that the
oxide is used in the isolation pad films as the barrier film for the well
implants. Using a selective hot phosphoric pad nitride etch or a chemical
downstream etch (CDE), the remaining pad oxide can be controlled to the desired
thickness for the CMOS device well implants. Specifically, the pad nitride can
be removed, leaving a well-controlled, uniform amount of oxide, to be used as
an implant screen.

Brief Summary Text - BSTX (20):
The present invention also improves seams, polysilicon-to-polysilicon shorts
yields, reduces the corner device leakage, and rounds the corners of the trench
isolations, all of which have significant MOSFET performance implications.

Drawing Description Text - DRTX (3):
FIGS. 1-9 illustrate a method of forming a semiconductor device, such as a
metal oxide semiconductor field-effect transistor (MOSFET), according to a
first preferred embodiment of the present invention, and more specifically FIG.
1 illustrates a step of forming isolations 4 in substrate 1 having a pad oxide
2 and a pad nitride 3 thereover, respectively;

Drawing Description Text - DRTX (17):
FIG. 15 is a graph illustrating the percent of STI TEOS fill remaining vs.
the conventional semiconductor device processing steps for both conventional
processing, and using the present invention.

Detailed Description Text - DETX (2):
The first preferred embodiment of the present invention eliminates the
transfer gate sacrificial oxide and the associated steps from the conventional

process as described above. Specifically, this process uses the initial pad oxide (e.g., the oxide in an isolation pad stack) as a screen film for the well implants. For instance, if this pad oxide is beneath nitride in a stack, using a selective, well-controlled wet (e.g., hot phosphoric acid etch) or dry etch (e.g., CDE), the nitride is removed, and the pad oxide is etched to the desired thickness to perform the well ion implants. Thus, the invention eliminates an entire oxide removal step, traditionally used to expose the Si substrate before forming desired thickness screens. This invented process will reduce significantly the corner divot, trench center pulldown, and synergistically reduce the chance of exposing STI trench voids which lead to polysilicon shorts in the isolation, as shown in a comparison of FIGS. 11 and 12, with FIG. 11 showing the results of the conventional techniques, and FIG. 12 showing the results of the present invention. As shown, the divot is reduced in size when the sacrificial oxide elimination process is used according to the present invention, and the trench corner Si is rounder than the conventional processes.

Detailed Description Text - DETX (5):
As shown in FIG. 2, the pad nitride 3 is stripped selectively to the pad oxide 2 to obtain the desired pad oxide thickness remaining. The range of desired thicknesses of the pad oxide 2 may be freely determined according to the MOSFET design constraints and requirements and thus is not limited by the present invention.

Detailed Description Text - DETX (8):
As shown in FIG. 6, the P-well mask 7 is stripped, for example, by ozone plasma, leaving the substrate with adjacent P-wells 8 separated by an N-well 6 and an isolation 4 (e.g., an STI or field oxide trench isolation). The pad oxide 2 is still present over the respective P-wells 8 and N-wells 6.

Detailed Description Text - DETX (12):
In FIG. 10, the polysilicon is etched at places other than under the mask 11, thereby to form the gates for the semiconductor device (e.g., MOSFET or the like).

Detailed Description Text - DETX (17):
As shown, with the present invention, by eliminating the traditional sacrificial oxide strip, the corners are more rounded on top of the isolation (e.g., STI or field oxide isolation), and the sharp pinching angles are noticeably absent. As a result, the oxide growth is more uniform, thereby providing enhanced insulation and preventing corner devices from activating at undesirably low voltages.

Detailed Description Text - DETX (21):
FIG. 15 is a graph illustrating the % TEOS remaining through STI conventional process steps. As shown, the most detrimental conventional process steps are sacrificial oxide and pad oxide strip (e.g., 40 and 60) for loss of isolation fill (e.g., as indicated by the steep slope). The elimination of the transfer gate sacrificial oxide conserves a net average of 8 percent loss of TEOS associated with the conventional processing step (sac oxide growth and strip).

Detailed Description Text - DETX (23):
Hence, instead of the pad oxide strip and the sacrificial screen oxidation step in the conventional process, the process according to the present invention uses the initial pad oxide as a barrier film for the well masks and implants. Using one selective, well-controlled pad nitride etch across the entire wafer, the pad oxide thickness can be controlled to the desired thickness for uniform well implants. Specifically, in STI processing the pad nitride may be removed by a hot phosphoric etch, and then the well implants may be performed directly through the pad oxide, with out any intermediate steps of

stripping the pad oxide, and growing a desired thickness oxide (e.g,. TG
sacrificial oxide).

Detailed Description Text - DETX (25):
For example, as mentioned above, the isolations are not limited to any one
type. Thus, the present invention is equally applicable to shallow trench
isolations (STIs) as well as to field oxide isolations (FOX) or the like. As
such, the present invention is transparent to STI or field oxide or the like
isolation processing.

Claims Text - CLTX (30):
17. The method according to claim 1, wherein a degree of ion implantation
during a well implantation is used to control a threshold voltage of said
device.

Current US Cross Reference Classification - CCXR (7):
438/297